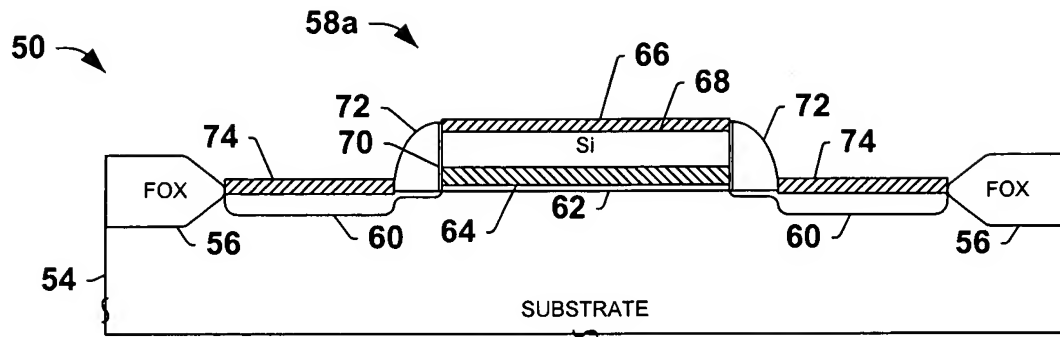
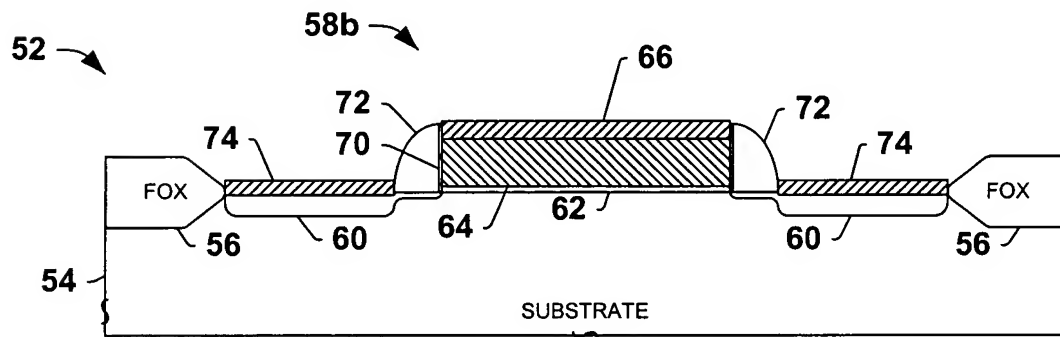


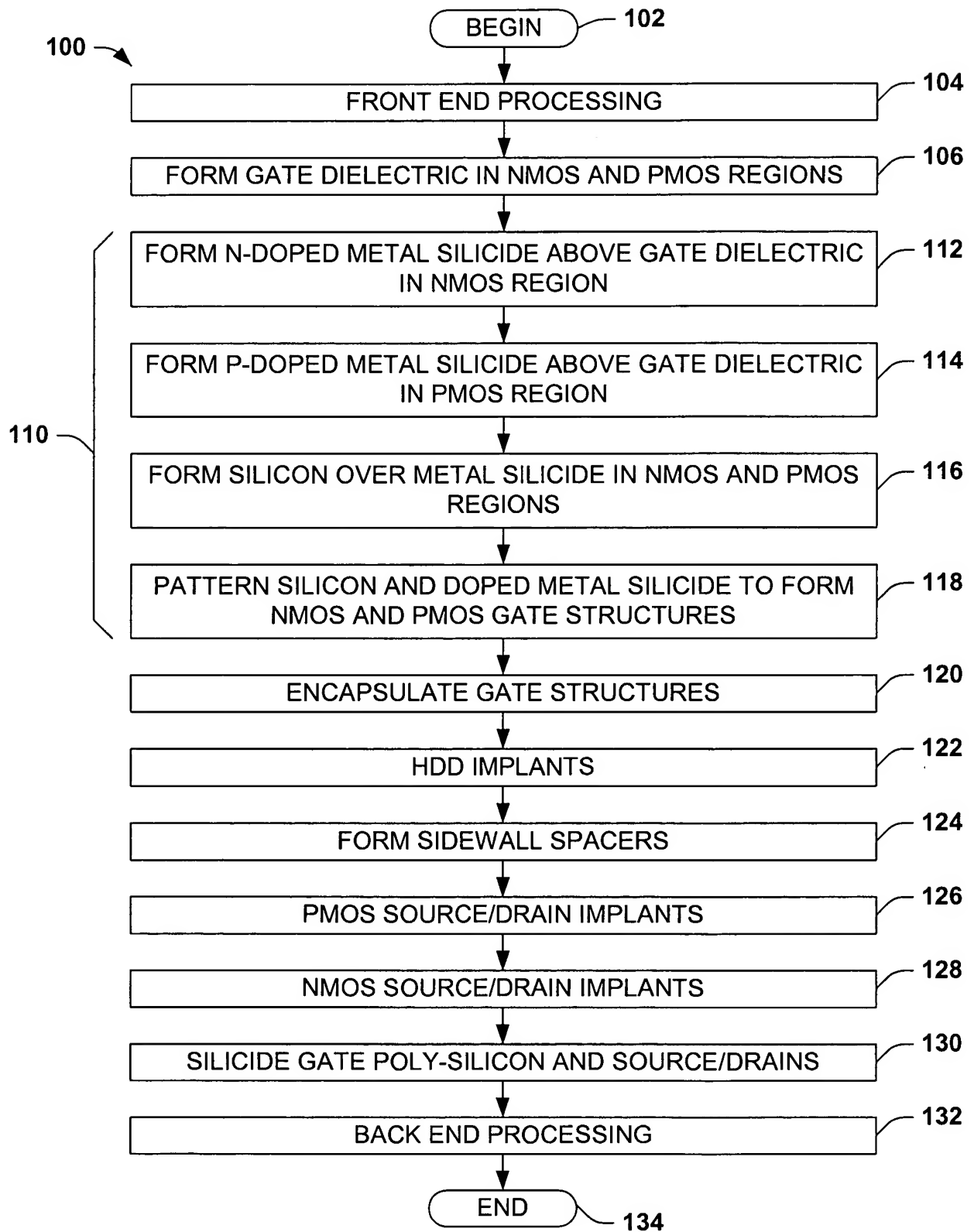
**FIG. 1**  
(PRIOR ART)



**FIG. 2A**



**FIG. 2B**



**FIG. 3**

110a

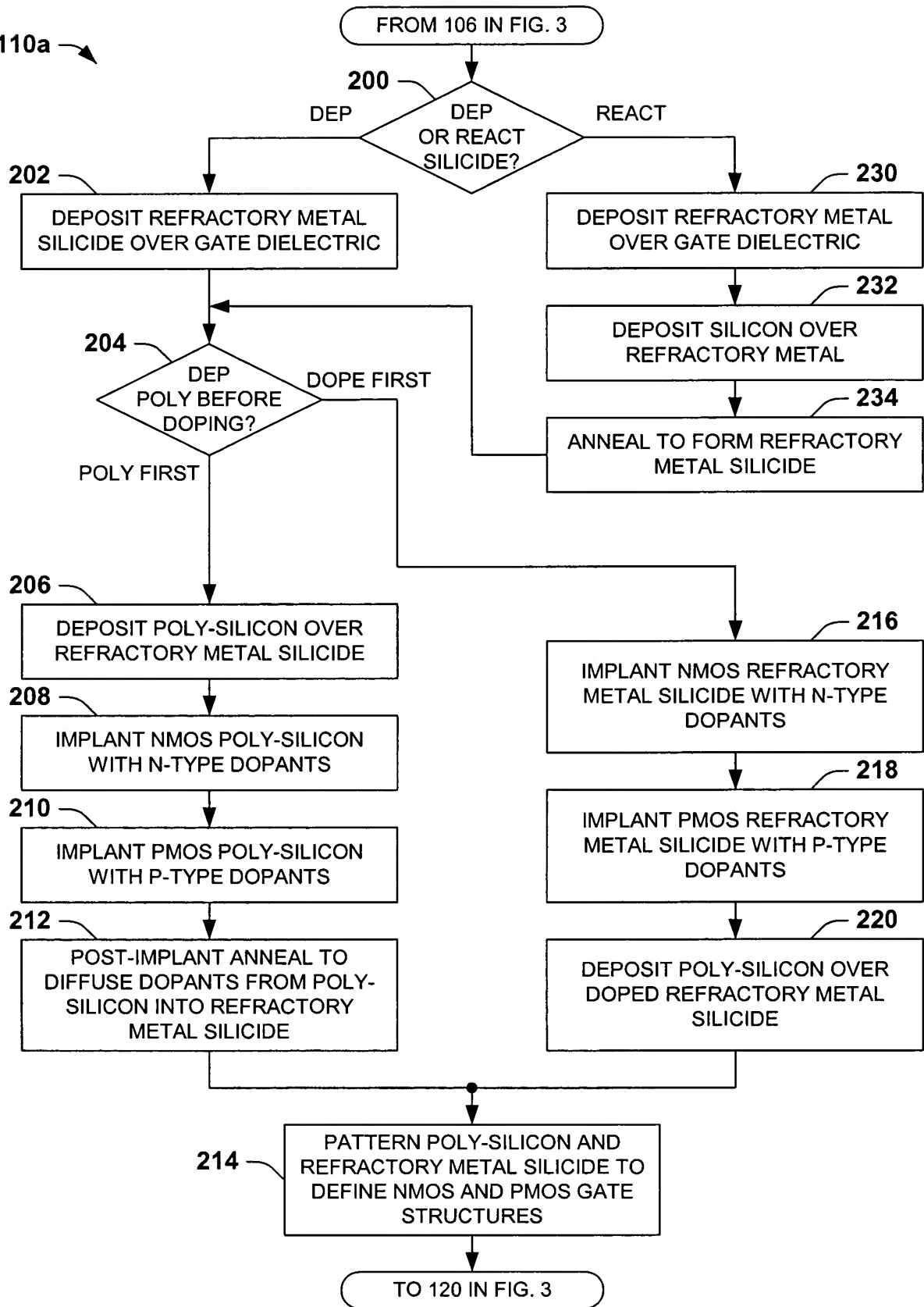
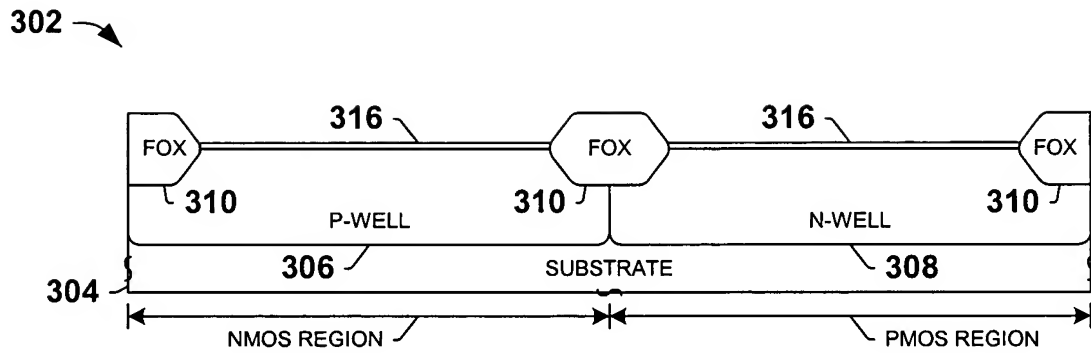
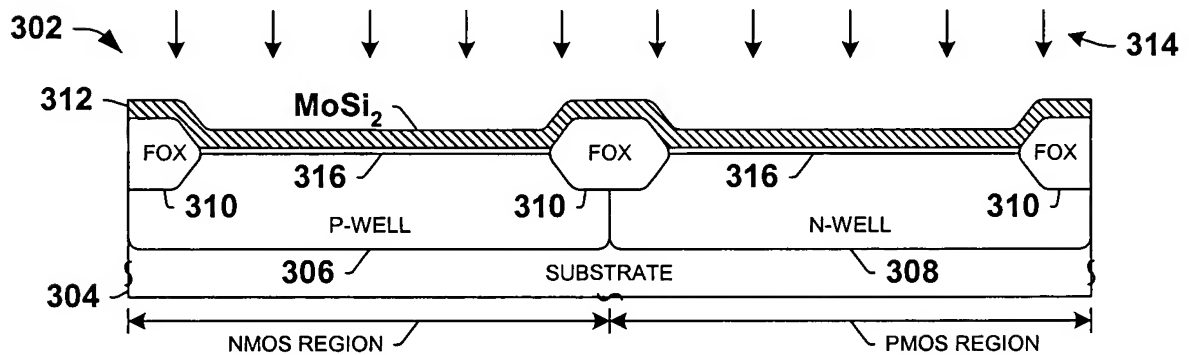


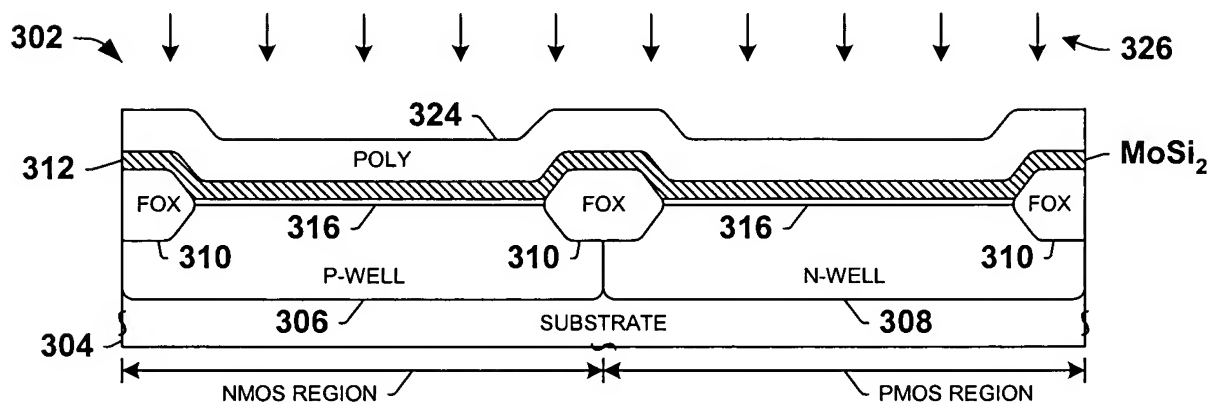
FIG. 4



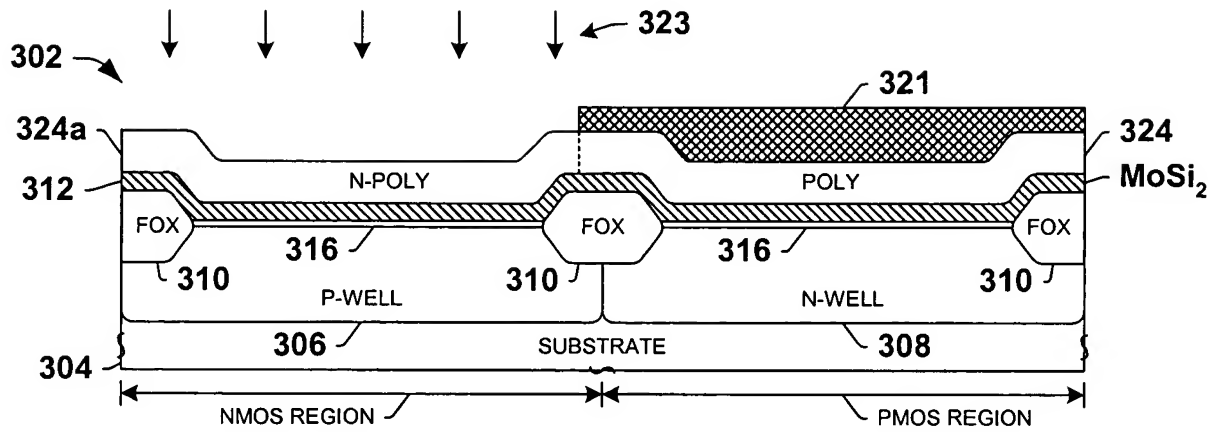
**FIG. 5A**



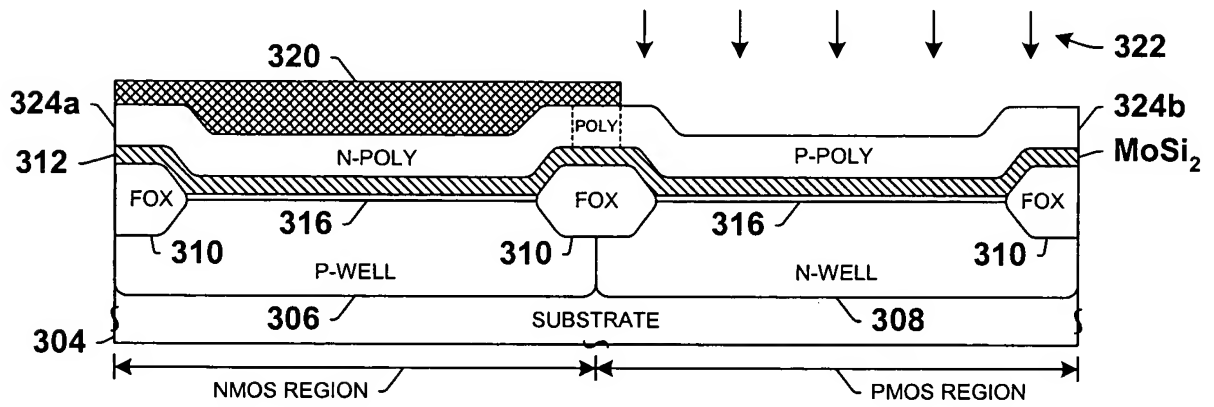
**FIG. 5B**



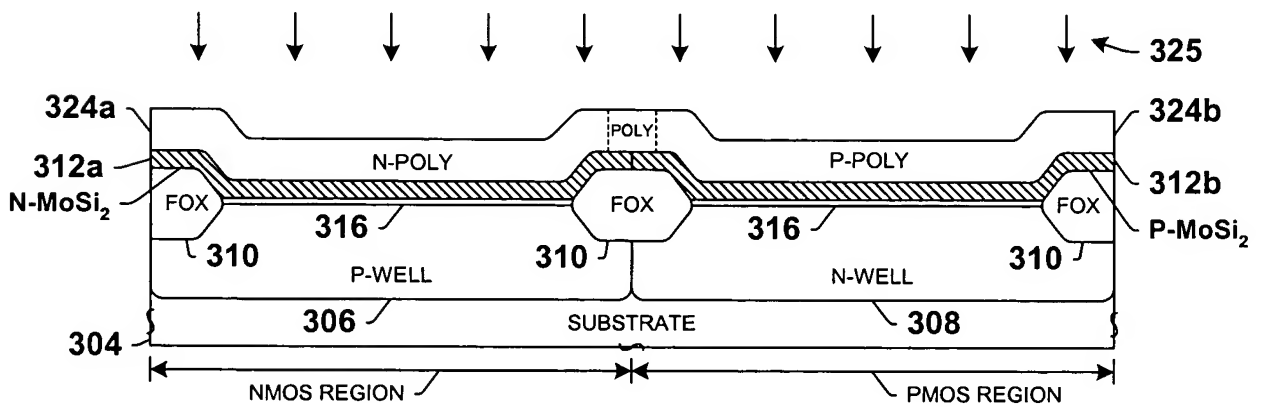
**FIG. 5C**



**FIG. 5D**



**FIG. 5E**



**FIG. 5F**

[illegible]

**FIG. 5I**

This cross-sectional view illustrates a semiconductor device with an NMOS region on the left and a PMOS region on the right, separated by a central gate structure. The device is built on a substrate 304. The NMOS region includes a P-WELL 306 and an N-POLY gate 341. The PMOS region includes an N-WELL 308 and a P-POLY gate 324b. Both regions feature FOX (field oxide) areas 310 and 312a/b, and a 332 layer. Arrows 343 indicate light incident on the top surface. Labels 302 and 306 point to the top and bottom of the NMOS region, while 308 points to the bottom of the PMOS region.

302

340 332 324a 344a 340 332 340 324b 344a 340 312b 344b

344b 312a N-POLY 344b 344b FOX 316 338 338 310 336 316 336 310 FOX

310 338 P-WELL 310 336 N-WELL 310

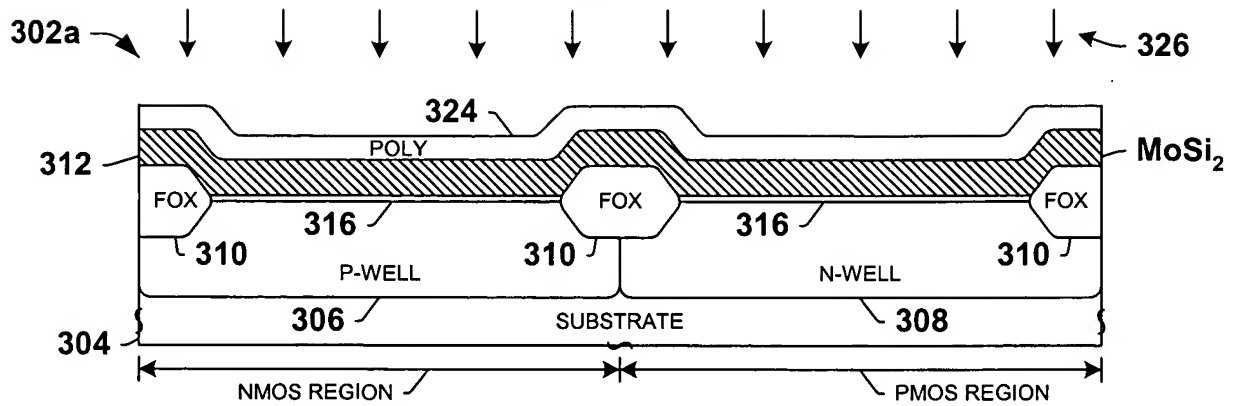
306 SUBSTRATE 308

304

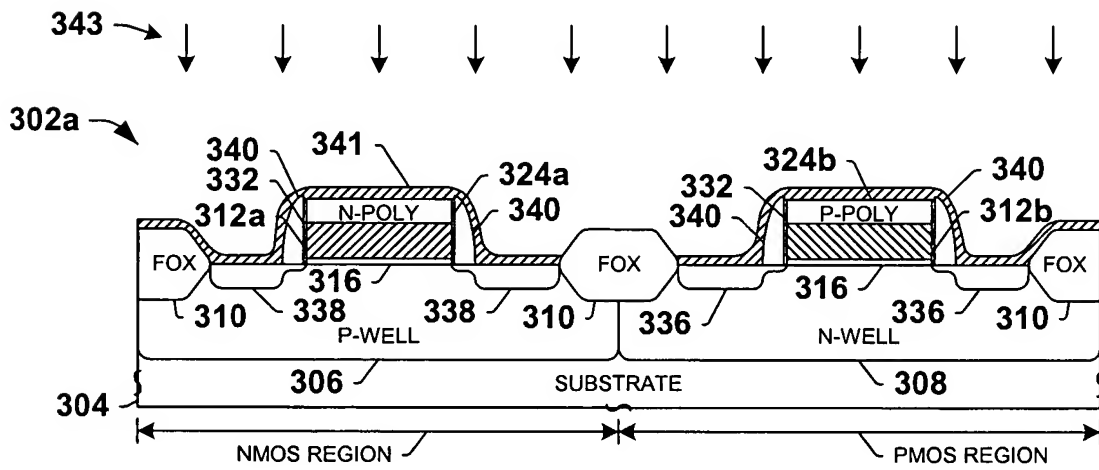
NMOS REGION PMOS REGION

**FIG. 5L**

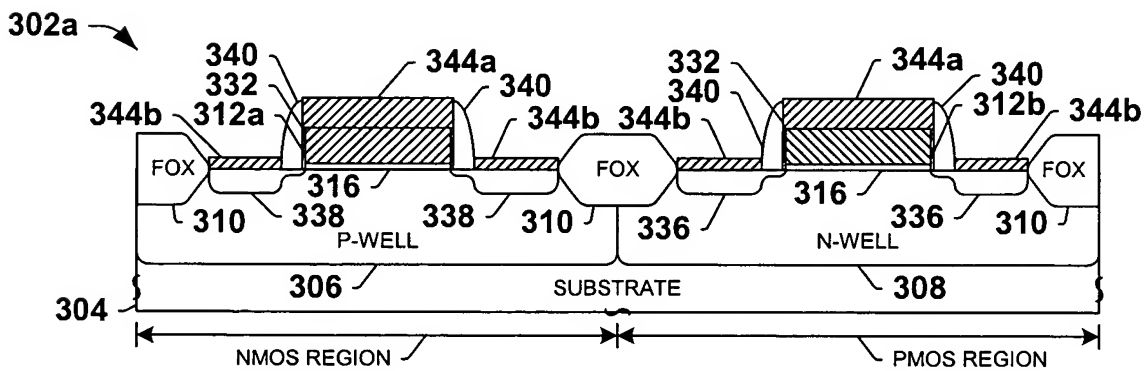




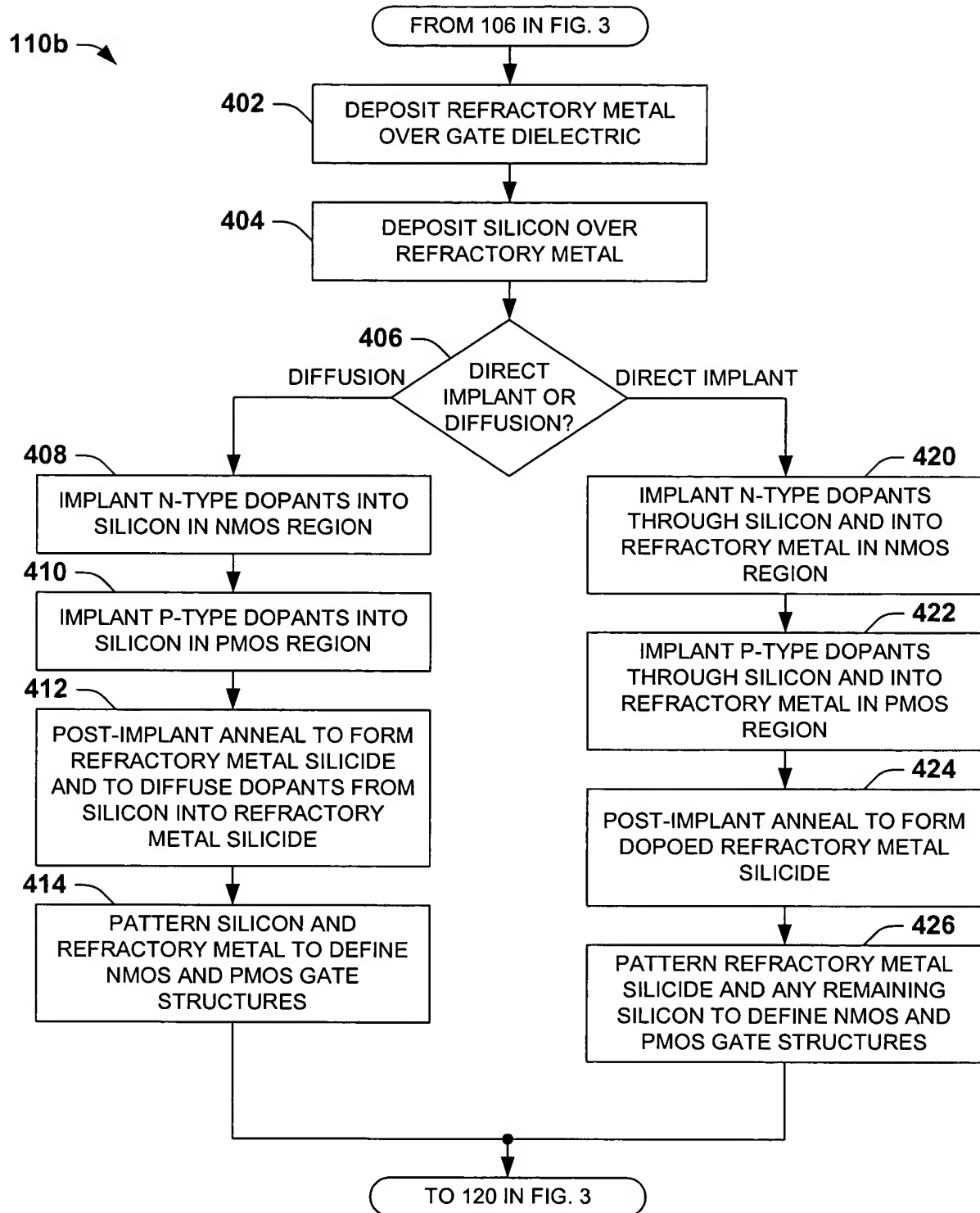
**FIG. 5M**



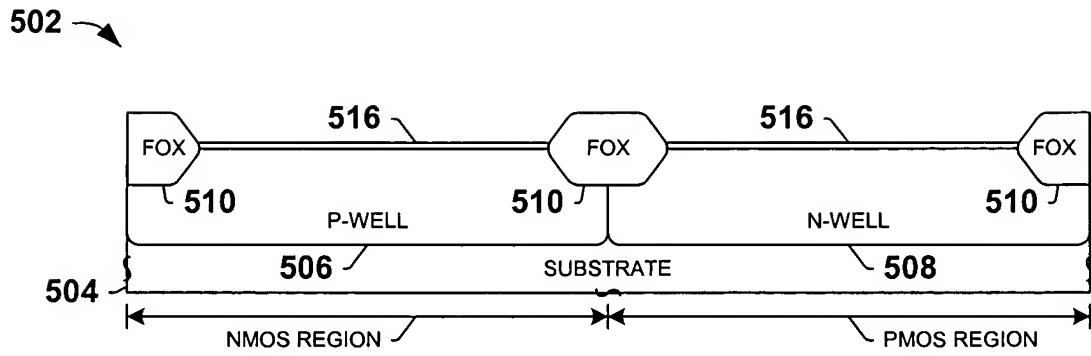
**FIG. 5N**



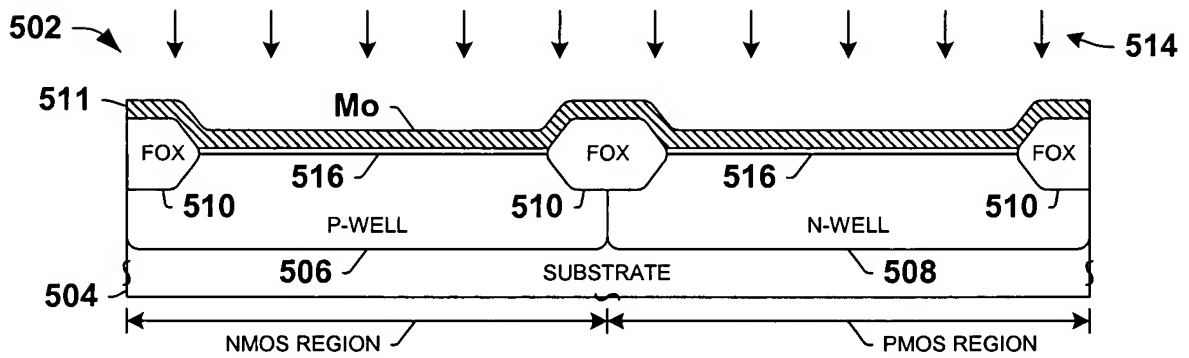
**FIG. 5O**



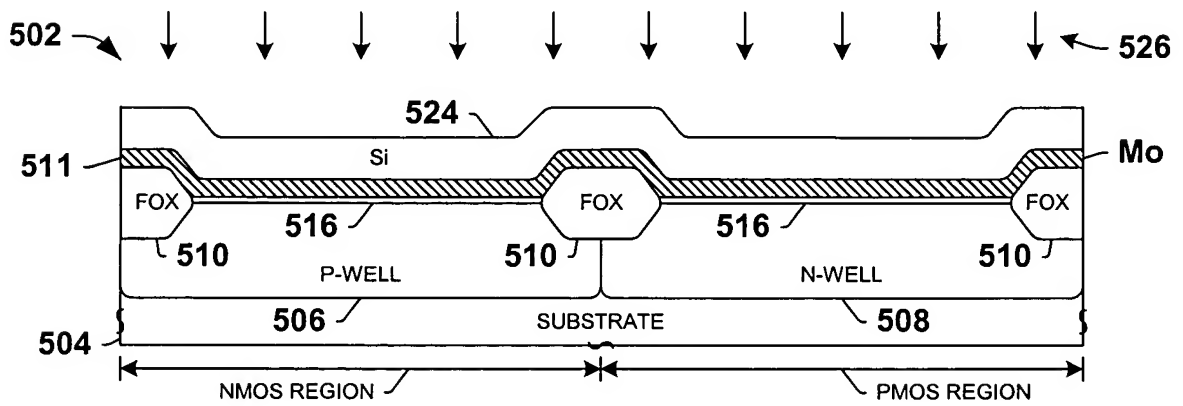
**FIG. 6**



**FIG. 7A**



**FIG. 7B**



**FIG. 7C**

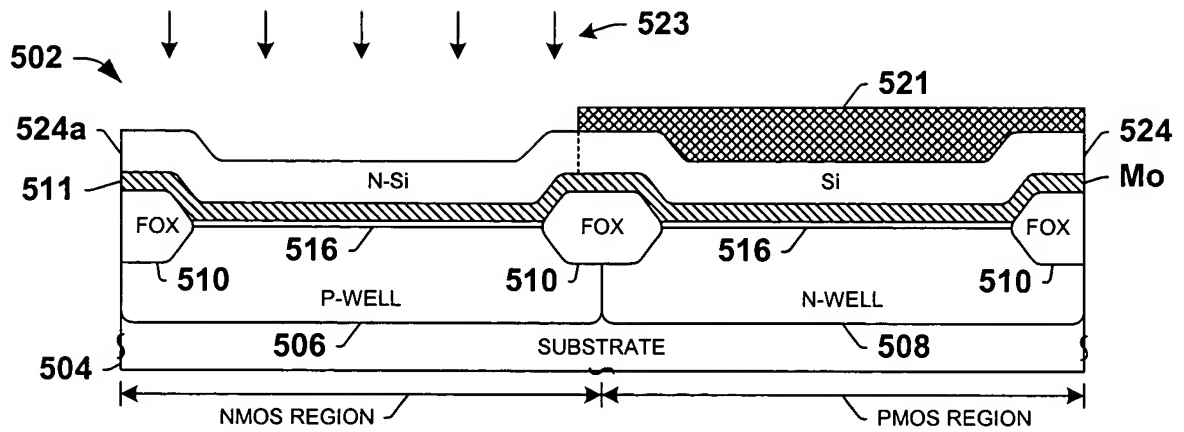


FIG. 7D

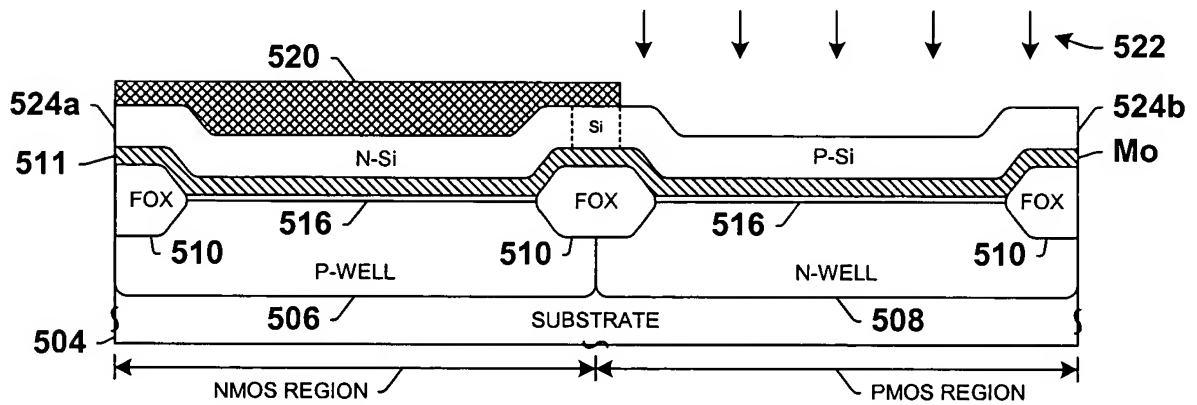


FIG. 7E

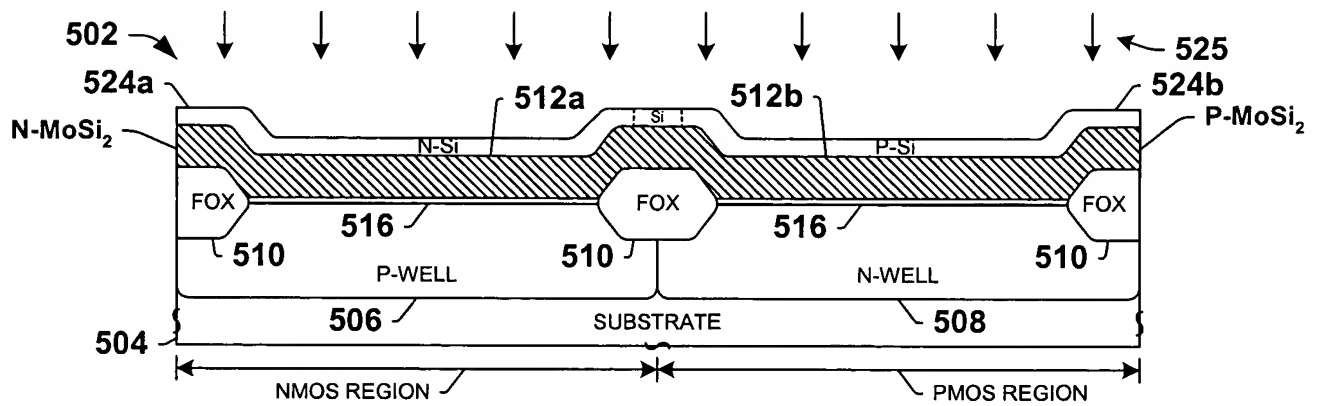
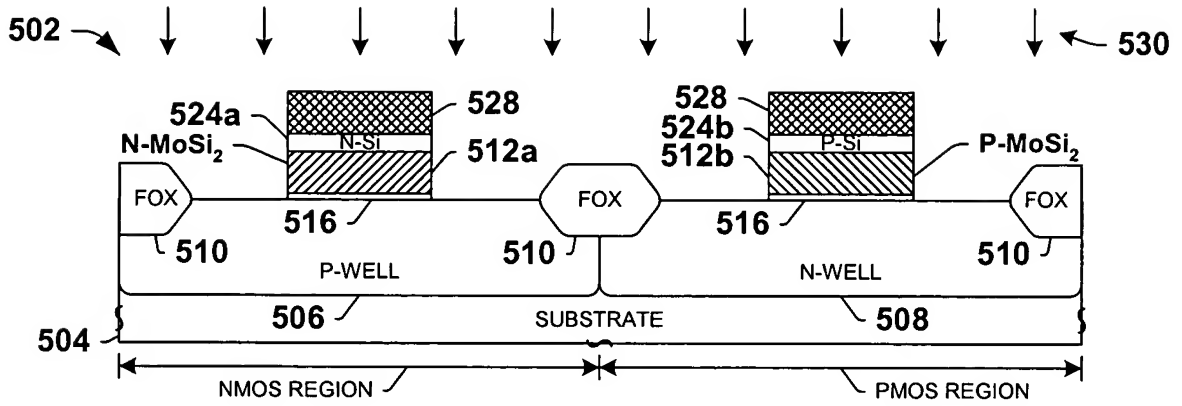
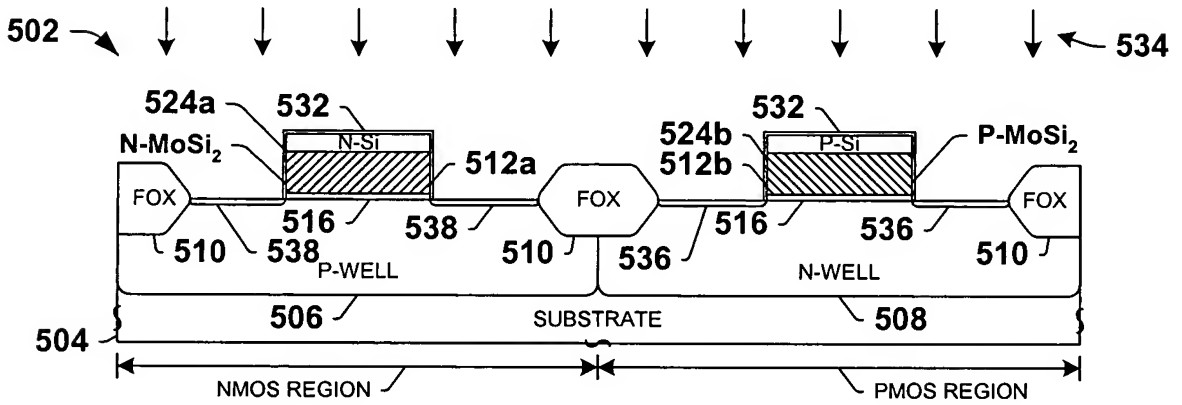


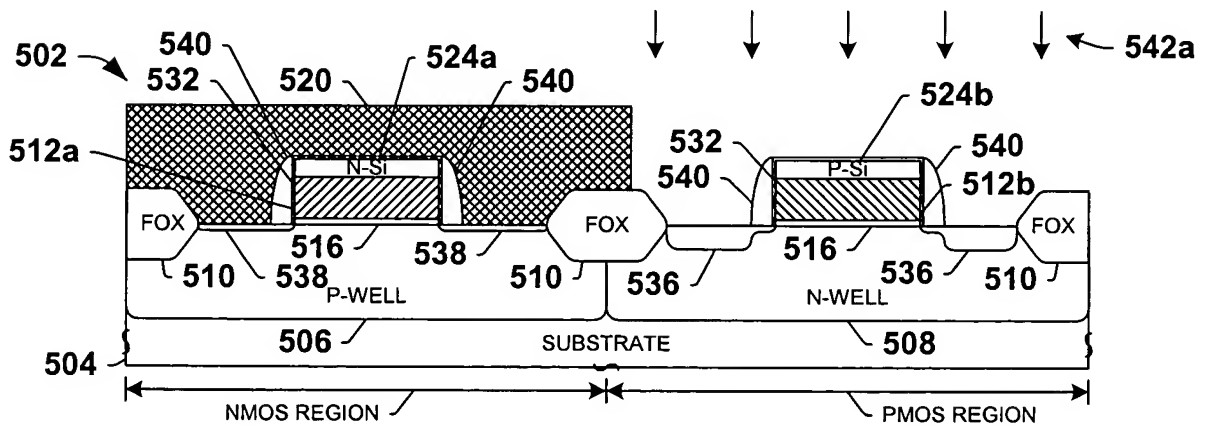
FIG. 7F



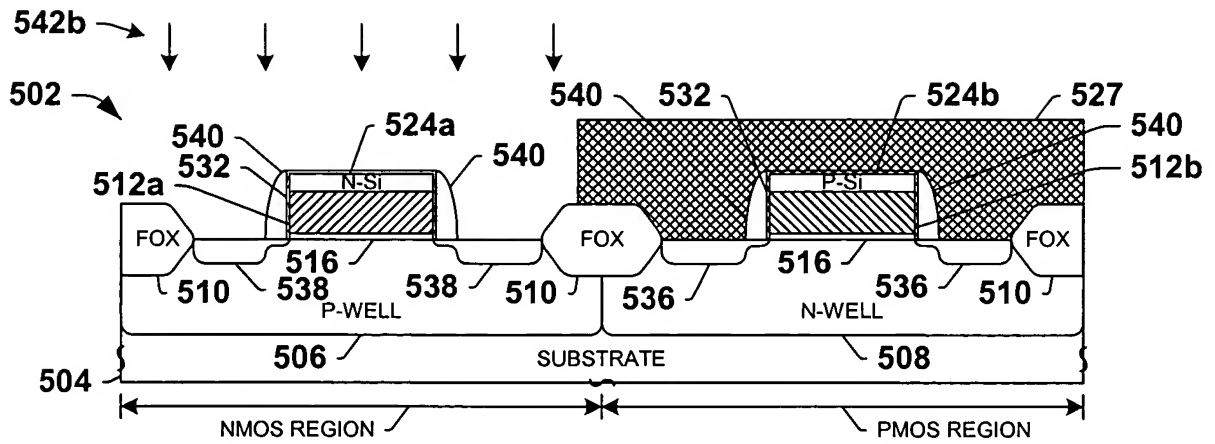
**FIG. 7G**



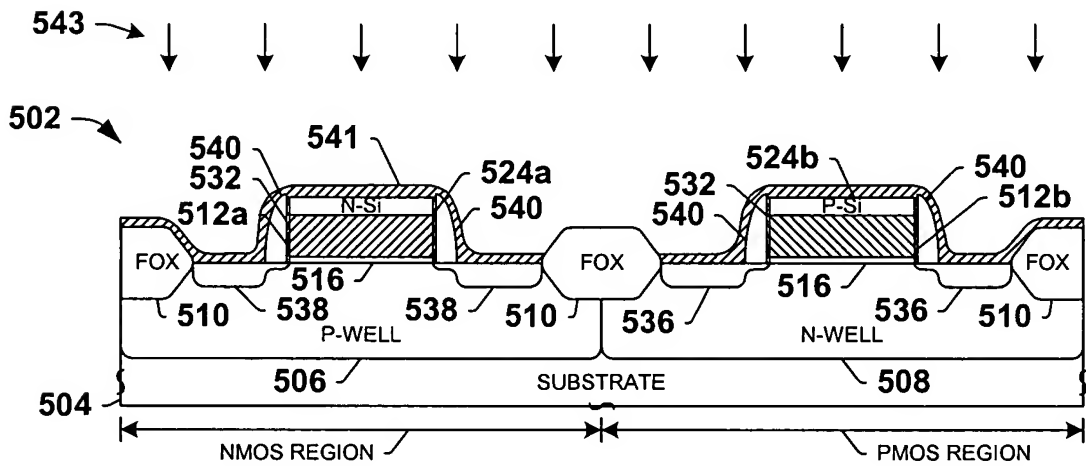
**FIG. 7H**



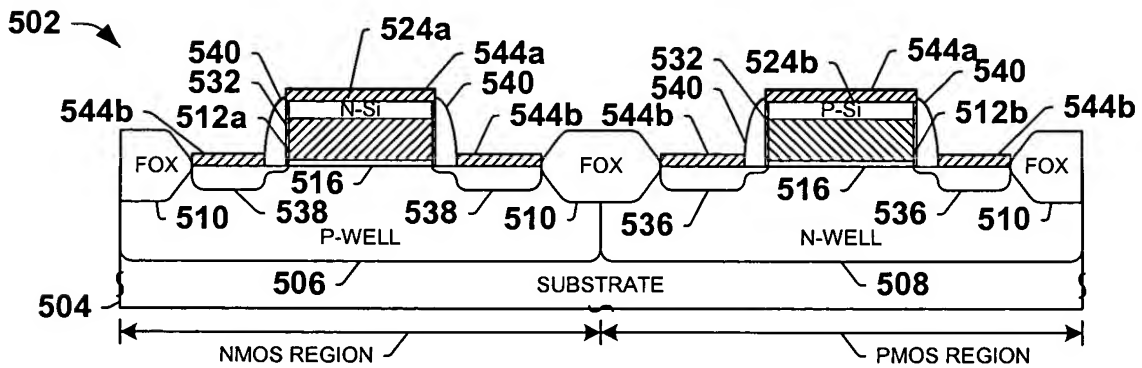
**FIG. 7I**



**FIG. 7J**



**FIG. 7K**



**FIG. 7L**

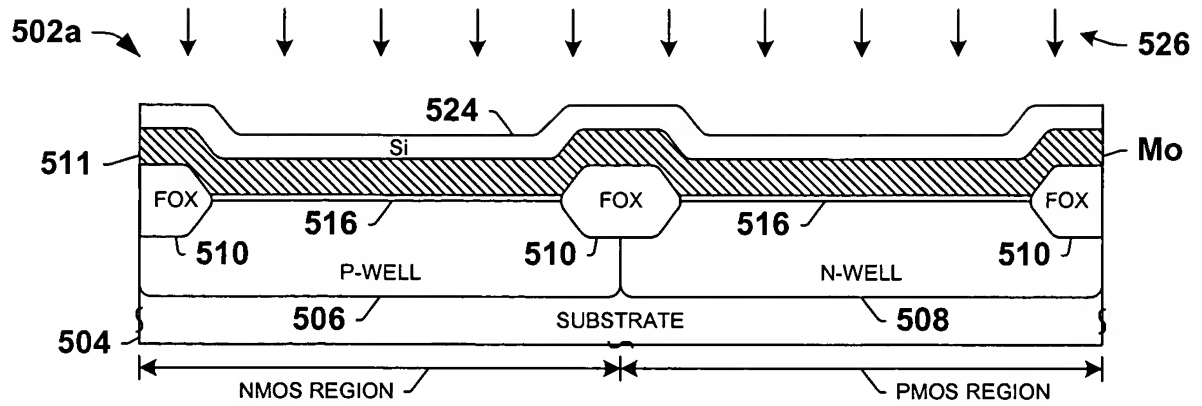


FIG. 7M

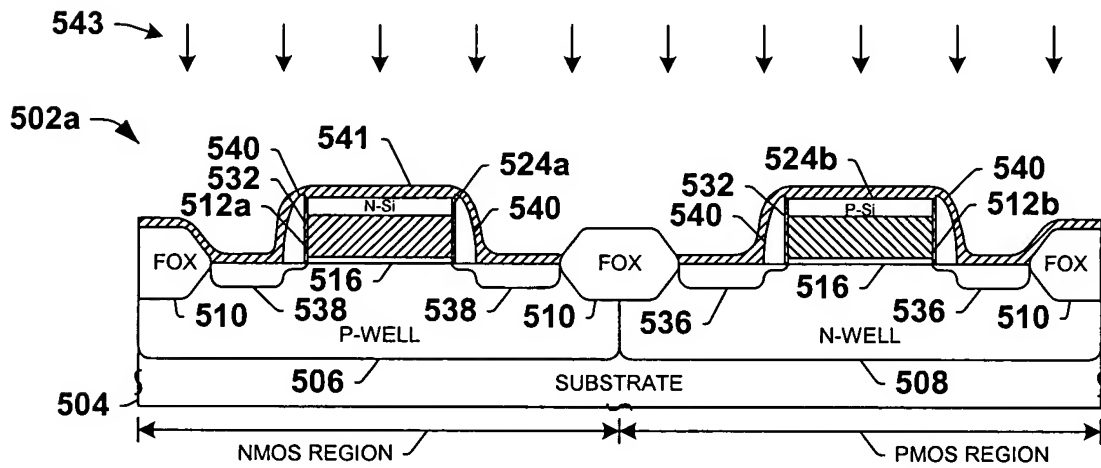


FIG. 7N

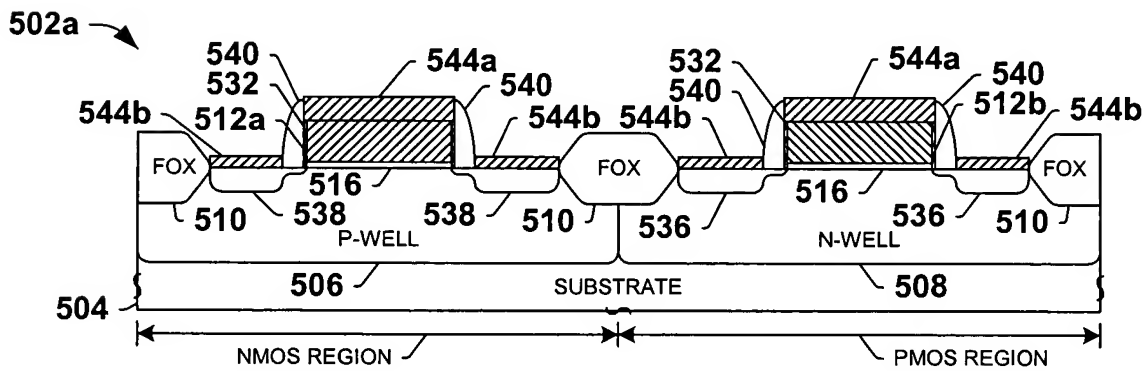


FIG. 7O